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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,500	07/08/2003	Matthew J. Adiletta	10559-075002 / P7567	8894
20985	7590	03/14/2006	EXAMINER	
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			ELLIS, RICHARD L	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/615,500	Applicant(s) ADILETTA ET AL.	
	Examiner Richard Ellis	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 36-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 36-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

1. Claims 36-41 remain for examination.
2. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

3. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.
4. Claims 36-41 are rejected under 35 USC § 103 as being unpatentable over Kogge, U.S. patent 5,475,856, in view of Agarwal et al., *APRIL: A Processor Architecture for Multiprocessing*, June 1, 1991.

Kogge taught (e.g. see figs. 1a-5) the invention substantially as claimed (as per claim 36), including a data processing ("DP") system comprising:

- A. a processor chip (col. 12 lines 23-29) comprising;
 - B. a reduced instruction set computer (RISC) core (fig. 1, 111, 113, "CONTROL UNIT", col. 5 lines 25-30); and,
 - C. multiple programmable units (fig. 1a, 111, 115 ... 111, 115, "DATA FLOW") communicatively coupled with the Reduced Instruction Set Computer core (111, 113, "CONTROL UNIT"), each of the respective multiple programmable units comprising a control store (col. 4 lines 38-42, "control unit"), an arithmetic logic unit (col. 4 lines 38-42, "data flow unit"), and storage for a program counter (col. 5 lines 19-20) associated with the thread executed by the respective programmable unit (col. 8 lines 51-55).
5. Kogge did not teach that the multiple programmable units were multithreaded, that the multiple programmable units contained storage for multiple program counters, or logic to re-enable availability for execution of one of the multiple threads in response to a signal associated with a memory reference issued by the thread. Agarwal et al. taught a multithreaded processor (pg. 3, section 3, first paragraph) that utilized multiple program

counters (pg. 3, section 3, second paragraph, "four sets of Program Counter (PC) chains") and included logic to reenable for execution a thread in response to a signal associated with a memory reference issued by the thread (pg. 1, second column, last paragraph, pg. 4, first column, section 3.1, second paragraph, pg. 4, second column, third paragraph, "the controller holds the processor until the request is satisfied"). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Agarwal et al. into the system of Kogge because Kogge taught that his system stalled upon accessing data located in a remote processor (col. 8 lines 58-67) and taught that it was important to minimize this latency (col. 8 line 67). Agarwal et al. taught an complementary system for tolerating the remaining delay after minimization by allowing the processor to context switch to another thread while the latency delay occurred (pg. 1, col. 1, abstract, first sentence, col. 1, section 1, first paragraph, pg. 10, section 8, first paragraph).

6. As to claim 37, both Agarwal et al. and Agarwal et al. taught that each multiple multi-threaded programmable unit comprised a programmable unit having a multi-stage instruction pipeline (Kogge states that his processing units are based on the RS/6000 RISC chip (col. 5 lines 27-30), a pipelined chip, and Agarwal et al. specifically states that his implementation is a pipelined system, pg. 3, col. 2, section 3, first sentence).
7. As to claims 38-39, they do not teach or define above the invention claimed in claims 36-37 and are therefore rejected under Kogge in view of Agarwal et al. for the same reasons set fourth in the rejection of claims 36-37, supra. As to the claimed feature of instructions to handle network protocol data path operations, Kogge taught that load/store instructions cause network communications (Kogge, col. 8 lines 58-67, Agarwal et al.) and as such are "network protocol data path operations for execution").
8. As to claims 40-41, they do not teach or define above the invention claimed in claims 36-39 and are therefore rejected under Kogge in view of Agarwal et al. for the same reasons set fourth in the rejection of claims 36-39, supra.
9. Applicant's arguments with respect to claims 36-41 have been considered but are

deemed to be moot in view of the new grounds of rejection.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Joy et al. taught a multiple CPU chip where each CPU was itself multi-threaded.

Gaetner et al. taught a system whereby individual processors can self schedule tasks to perform.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
March 9, 2006



RICHARD L. ELLIS
PRIMARY EXAMINER